Surface Mount Instructions for QFN / DFN and LGA Laminate Packages

Rev. V14

Introduction

The layout of the surface mount board plays a critical role in product design and must be done properly to achieve the intended performance of an integrated circuit. An accurate PCB pad and solder stencil design provides a proper connection interface between the IC package and the board. With the correct pad geometry, the package will self-align when subjected to a solder reflow process and will also allow for just enough excess surface area for adequate solder filleting. The solder mask should be applied over bare copper (SMOBC) to avoid solder reflow under the solder mask.

These considerations apply in general for most of MACOM's surface mount packaged IC's. This application note provides specific guidelines for mounting quad flat no-leads packages (QFN per JEDEC MO-220), and dual flat no-leads packages (DFN per JEDEC MO-229).

PCB Pad Design

The first consideration in mounting the QFN / DFN to a board is the layout of metalized pads. The US-based trade association, IPC, has developed land pad design standards contained in the document IPC-SM-782 entitled *Surface Mount Design and Land Pattern Standards*.

Figures 1-1 through 1-3 shows the PCB geometry developed for MACOM's QFN / DFN packages based on the general guidelines contained within IPC-SM-782. The center area or the thermal pad, acts as an RF ground pad and thermal path to conduct heat away from the package. Normally, the size of the thermal pad should match the size of the exposed pad on the bottom of the package. However, a smaller thermal pad is sometimes recommended to prevent solder bridging to the lead pads. Table 1 shows some suggested PCB pad dimensions for QFN / DFN packages used by MACOM. The solderable length of the lead pad is controlled by the solder mask opening (Lm) as indicated in Table 2, in combination with pad length (L) as indicated in Table 1.

Via Design

To improve the thermal/RF performance of the package, we recommend providing thermal vias on the PCB. These vias provide a heat transfer and RF ground path from the top surface of the PCB to the inner layers and the bottom surface. We recommend a via diameter of 0.3 mm in a 1.0 mm pitch array for standard square packages. This is shown in Figure 1-1, in which the vias are 1.0 mm away from their diagonal neighbors. Other non-standard designs may require a slightly different via diameter and pitch as shown in Figures 1-2, 1-3, and 2-4. The vias should have 1 oz copper plating inside the via and then should be subsequently filled and plated over. Depending on the product performance requirements for thermal dissipation and the overall thickness of the substrate, the vias can be either conductively filled, non-conductively filled or solid copper. Thinner substrates(ie < .6 mm) allow for the opportunity to use a solid copper process for better thermal dissipation however this should be verified with the fabricator for the substrate. For optimal thermal performance refer to the specific product datasheet for via pattern recommendations.

Figure 1-1 PCB Land Design

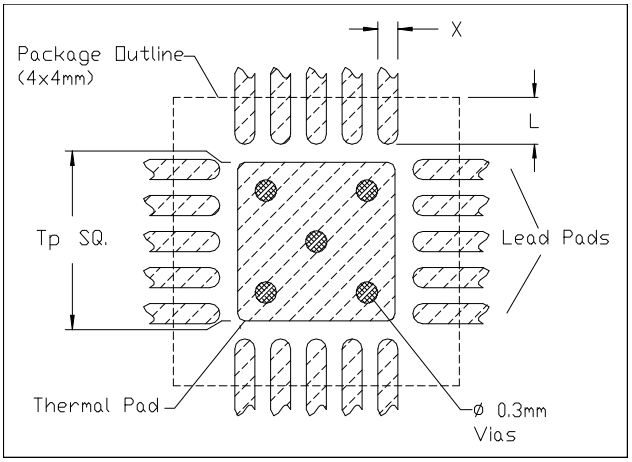

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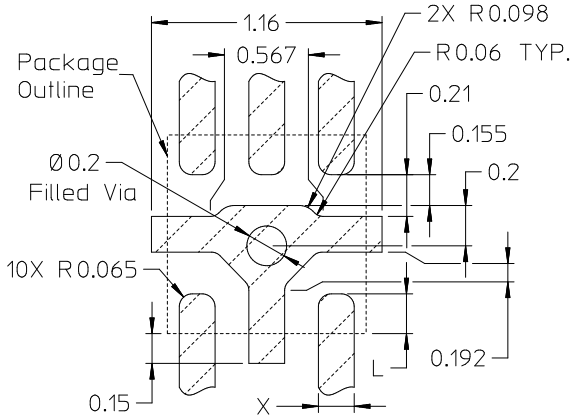
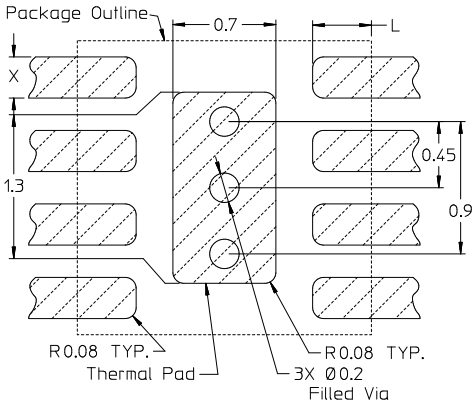
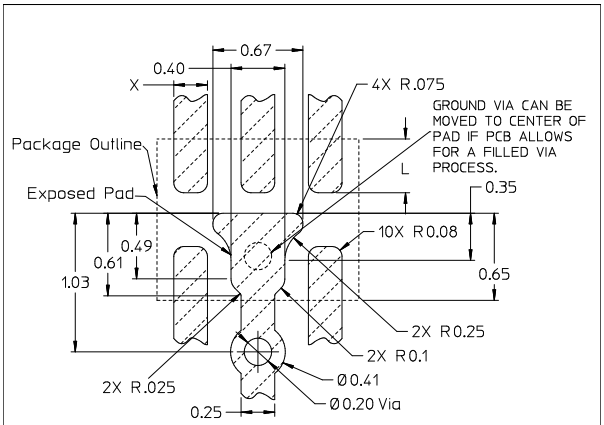
Figure 1-2 PCB Land Designs



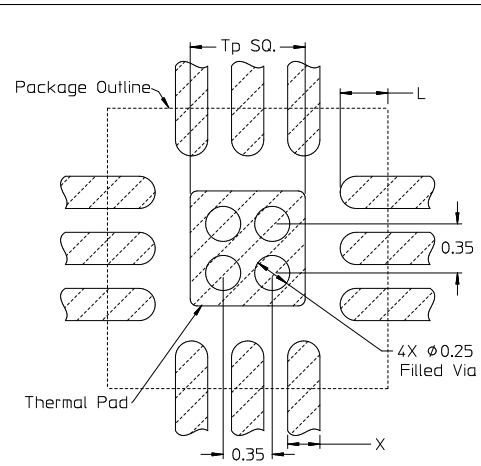
1 x 1 mm X1-DFN - 6LD



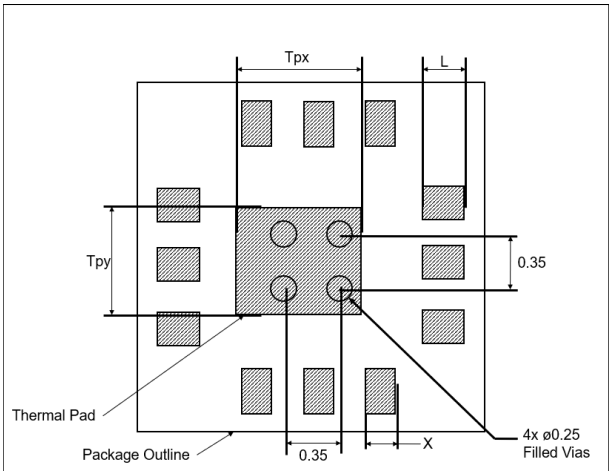
2 x 2 mm PDFN - 8LD



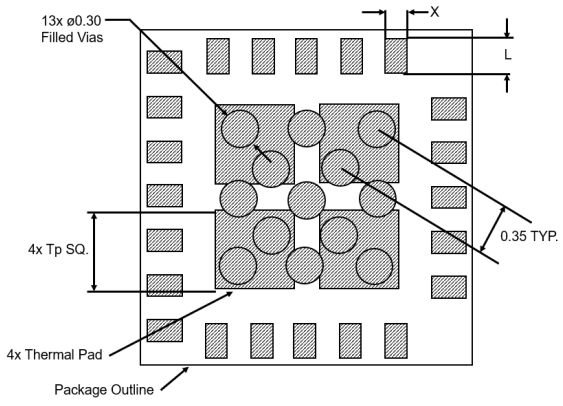
1.2 x 1.5 mm PDFN/TDFN - 6LD



2 x 2 mm STQFN - 12LD



2.25 x 2.25 mm LGA - 12LD



3 x 3 mm LGA - 22LD

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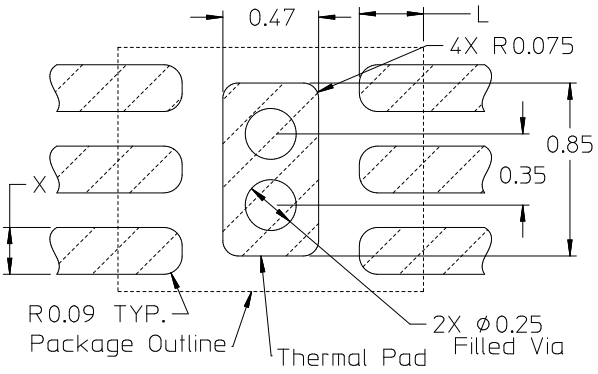
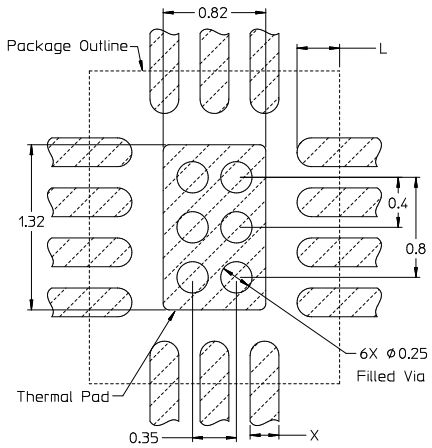
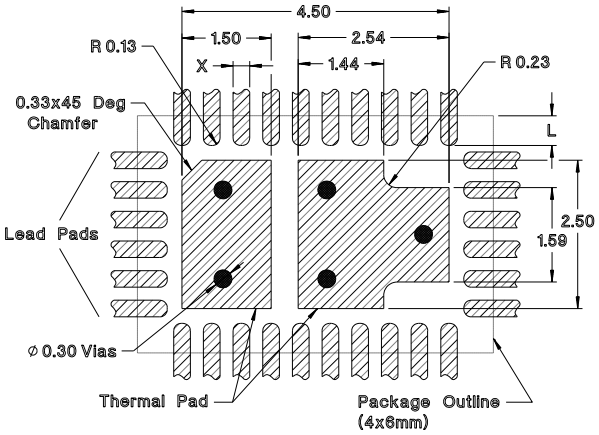
Figure 1-3 PCB Land Designs - cont.



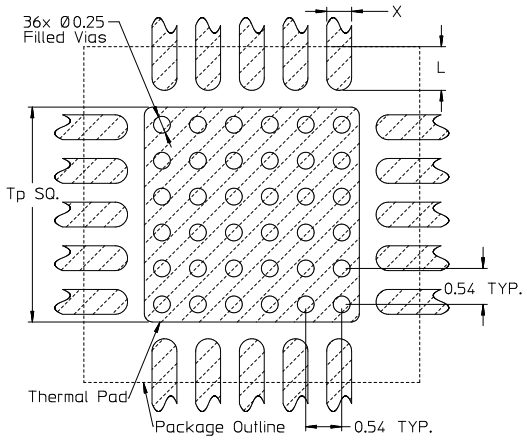
1.5 x 1.2 mm TDFN - 6LD



2 x 2.5 mm STQFN - 14LD



4 x 6 mm PQFN - 32LD



5 x 5 mm PQFN - 20LD (Power Amp)

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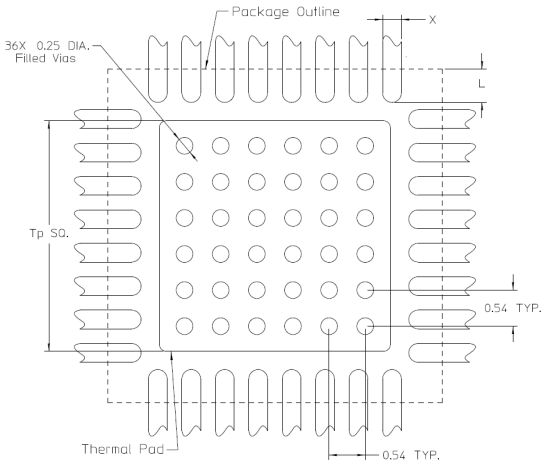
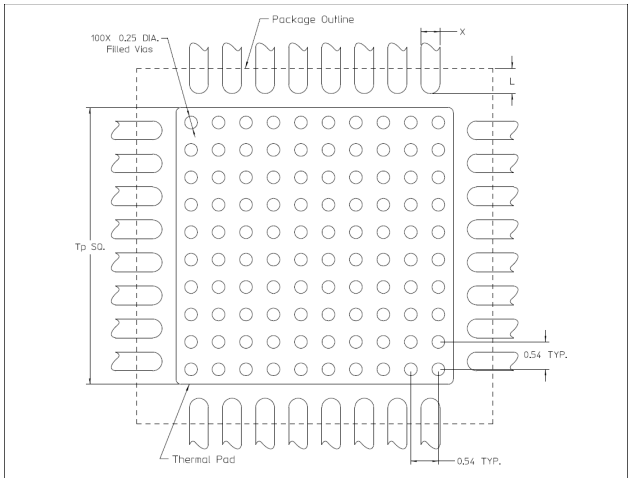
Figure 1-3 PCB Land Designs - cont.



5 x 5 mm PQFN - 32LD



7 x 7 mm PQFN - 32LD

Table 1. Recommended PCB Land Pattern Dimensions

Package Description				PCB Land Pattern Dimensions (mm)			Max # of Vias
Package Type	Size (mm)	No. of Leads	Lead Pitch (mm)	Tp	X	L	
X1-DFN	1 x 1	6	0.35	Fig. 1-2	0.18	0.20	1
TDFN	1.2 x 1.5	6	0.50	Fig. 1-2	0.25	0.40	1
TDFN	1.5 x 1.2	6	0.40	Fig. 1-3	0.23	0.315	2
PDFN	2 x 2	8	0.50	Fig. 1-2	0.28	0.40	3
STQFN	2 x 2	12	0.40	0.82	0.23	0.34	4
STQFN	2 x 2.5	14	0.40	Fig.1-3	0.23	0.34	6
LGA	2.25 x 2.25	12	0.40	0.8 x 0.7	0.20	0.275	4
LGA	3 x 3	22	0.40	0.7	0.20	0.25	13
PQFN	3 x 3	12	0.50	1.2	0.28	0.65	2
PQFN	3 x 3 (1.45 mm Exp. Pad)	16	0.50	1.5	0.28	0.50	2
PQFN	3 x 3 (1.7 mm Exp. Pad)	16	0.50	1.6	0.28	0.45	2
PQFN	4 x 4	16	0.65	2.2	0.37	0.65	5
PQFN	4 x 4	20	0.50	2.2	0.28	0.65	5
PQFN	4 x 4	24	0.50	2.55	0.28	0.50	5
PQFN	4 x 6 (V1)	32	0.50	Fig. 1-3	0.28	0.50	5
PQFN	5 x 5 (std)	20	0.65	3.2	0.37	0.65	9
PQFN	5 x 5 (Power Amp.)	20	0.65	3.2	0.37	0.65	Fig.1-3
PQFN	5 x 5	28	0.50	3.2	0.28	0.65	9
PQFN	5 x 5	32	0.50	3.45	0.28	0.50	Fig.1-3
PQFN	6 x 6	28	0.65	4.5	0.40	0.50	18
PQFN	7 x 7	32	0.65	5.45	0.37	0.50	Fig.1-3

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Solder Mask Considerations

The solder mask, a permanent part of most PCB's applied after etching the metal pads, helps protect the spaces between the metal pads from solder paste and unintended adhesion of solder. All metalized pad areas on a printed circuit board can be classified as either solder mask defined (SMD) or non-solder mask defined (NSMD), depending on the size of the opening in the solder mask relative to the size of the metal pad.

An SMD metal pad has its periphery partly covered by the solder mask. An NSMD metal pad sits within a larger opening in the solder mask.

The copper etching process used to define metal pads provides tighter control than the solder mask process, so MACOM recommends using NSMD pads whenever possible. The recommended solder mask opening for all lead pads should be 140 microns larger than the pad size, which results in 70 microns clearance between the copper pad and solder mask. For example, the 4 x 4 mm 20-lead package has an indicated width of the PCB lead pad (X) of 0.28 mm (Table 1) and the width of the solder mask opening (Wm) would be 0.42 mm (Table 2). In the other direction, the length of the solder mask opening (Lm) should be 180 microns extended outward from the edge of the package and 70 microns inward from the PCB pads, which results in a total length of 900 microns (see Table 2).

To avoid any solder bridging between the thermal pad and lead pads, we recommend making the thermal pad an SMD pad so that the solder mask defines the thermal land. The mask opening (Tm) should be 100 microns smaller than the recommended thermal land size, which would be 2.1 mm for the 4 mm PQFN package. See Table 2 for additional recommended thermal land solder mask opening dimensions.

To prevent solder wicking inside the via during reflow, we recommend solder mask pads over all thermal via areas. The solder mask diameter should be 100 microns larger than the via diameter. Based on our experience with suppliers, we have found fewer voids under the die paddle using solder mask printing on the top surface of the PCB, as compared with solder mask printing on the bottom. Filled vias also work well as an alternative to solder mask to further enhance thermal conduction for high power amplifier products (see figure 1-3). These printed boards should also include 1 oz. copper plating in vias which are subsequently filled with a conductive via fill material and then over-plated. It is recommended that there be 2 oz. final copper thickness on the thermal pad for optimal heat transfer.

Application Note

Figure 2-1 Solder Mask Designs

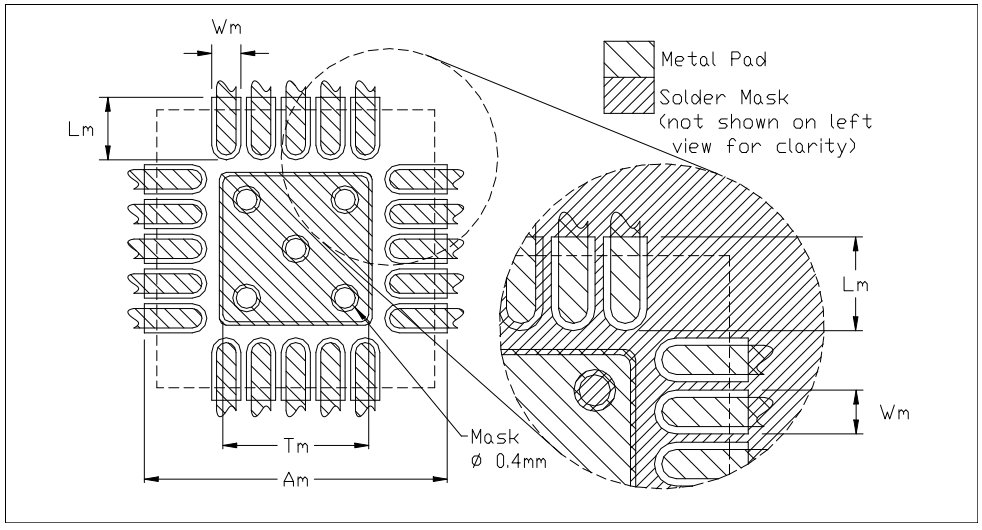

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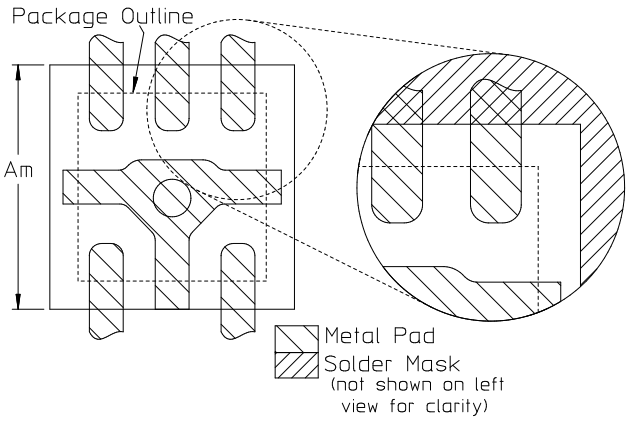
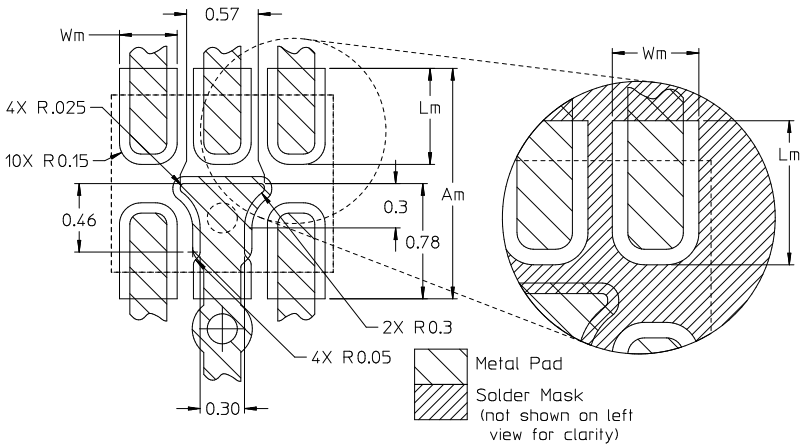
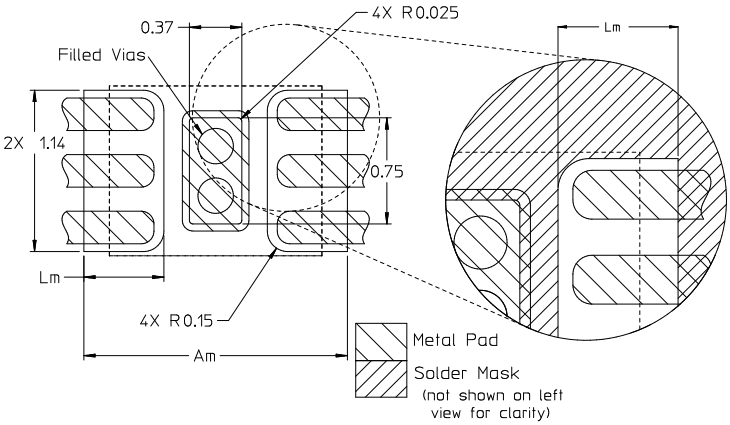
Figure 2-2 Solder Mask Designs



1 x 1 mm X1-DFN - 6LD



1.2 x 1.5 mm PDFN/TDFN - 6LD



1.5 x 1.2 mm TDFN - 6LD

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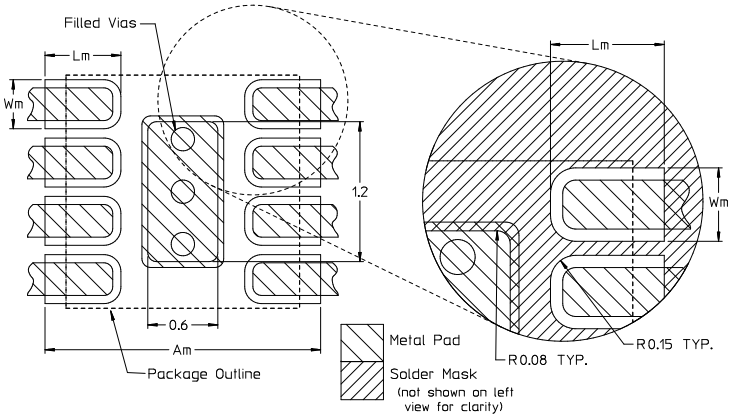
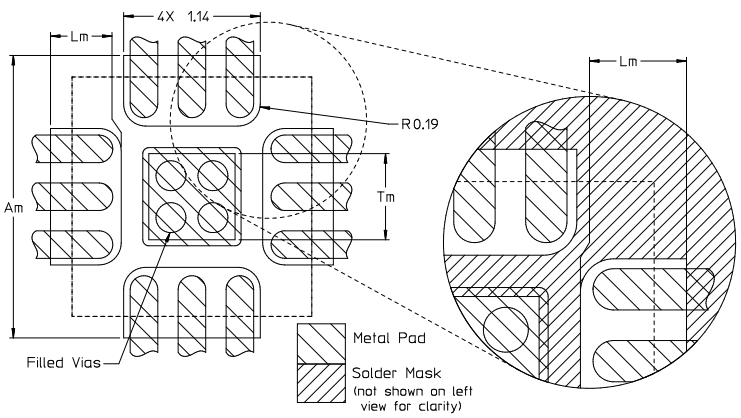
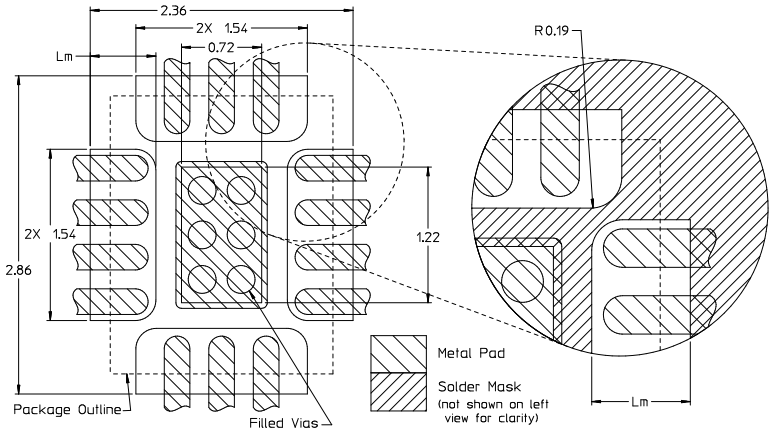
Figure 2-3 Solder Mask Designs - cont.



2 x 2 mm PDFN - 8LD



2 x 2 mm STQFN - 12LD



2 x 2.5 mm STQFN - 14LD

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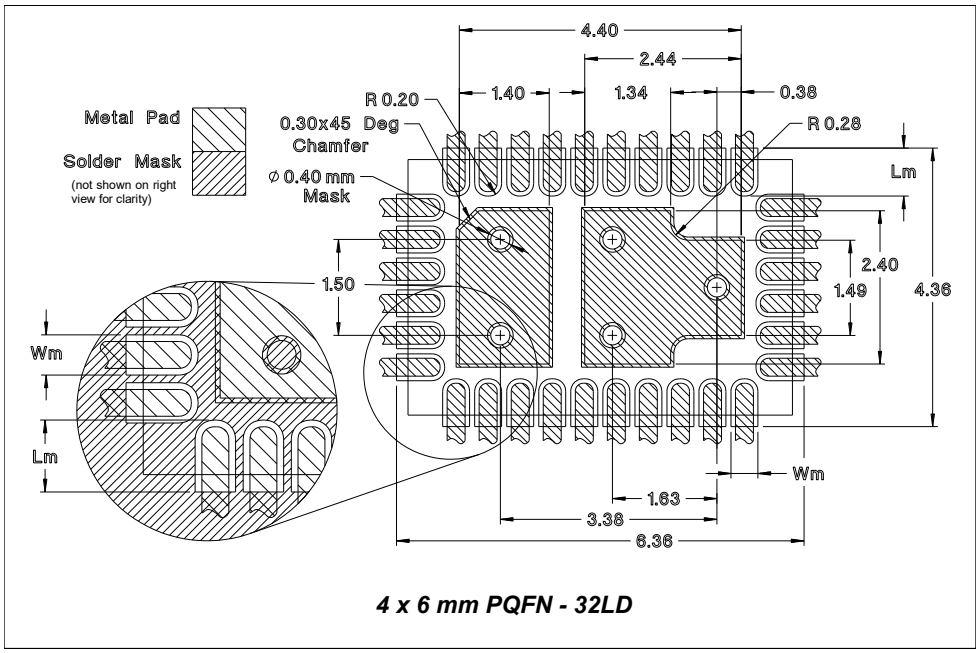
Figure 2-4 Solder Mask Design - cont.



4 x 6 mm PQFN - 32LD

Stencil Design

A stencil is used for applying solder paste to the PCB. Although the PCB design suggested in Figures 1 through 2 will help eliminate some surface mounting difficulties, special considerations apply in stencil design and solder paste printing for both lead pad and thermal pads.

Surface mount processes vary from company to company, so we recommend careful development of your process for QFN / DFN packages. The following provides some guidelines for stencil design.

We recommend a stencil thickness of 0.100 to 0.125 mm for fine pitch packages (0.5 mm or smaller). This thickness can be increased to 0.15 mm for coarser pitch parts. A laser-cut, stainless steel stencil with electro-polished trapezoidal walls is recommended.

The stencil opening for all lead pad areas should be the same as the pad size on the PCB (Tables 1 & 2). As mentioned before, the function of the thermal pad is to allow for heat removal from the package as well as providing an effective RF ground. Therefore, a good stencil design becomes important for getting an optimal solder paste distribution between the lead pads and the thermal pad. To minimize voids and defects, use smaller multiple stencil openings for the thermal pad instead of one big opening. Figures 3-1 through 3-3 shows the recommended stencil designs. The target coverage for solder paste area is to maintain 50 to 80 percent of the overall thermal pad area. The selected web width is 0.2 mm running across the vias as shown in Figures 3-1 through 3-3.

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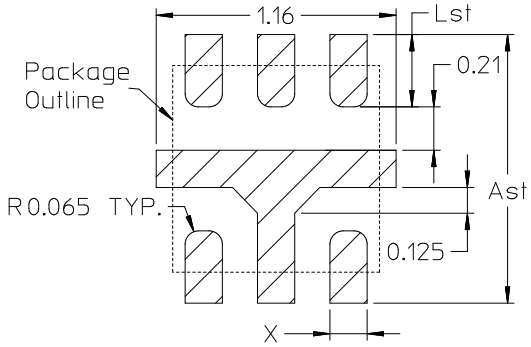
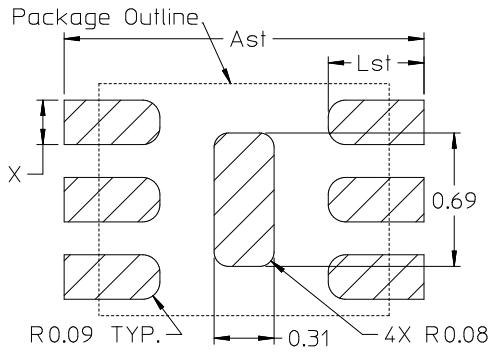
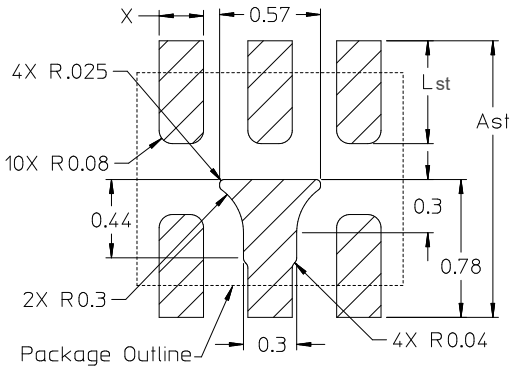
Figure 3-1 Stencil Designs



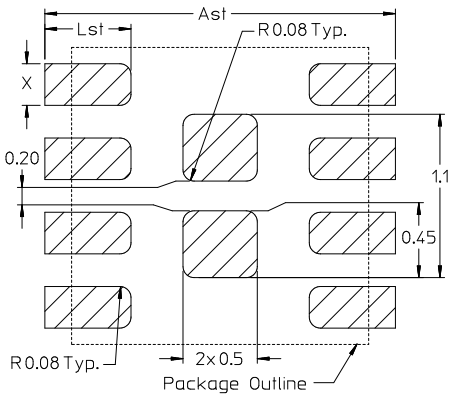
1 mm X1-DFN - 6LD



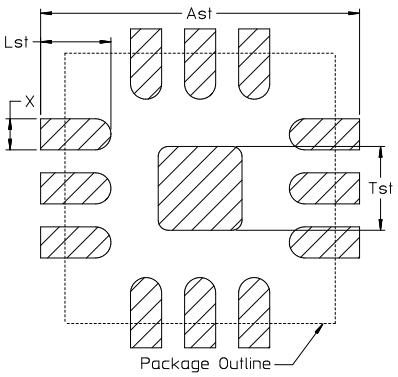
1.5 x 1.2 mm TDFN - 6LD



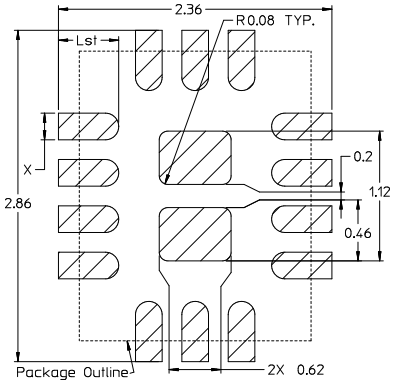
1.2 x 1.5 mm PDFN/TDFN - 6LD



2 mm PDFN - 8LD



2 mm STQFN - 12LD



2 x 2.5 mm STQFN—14LD

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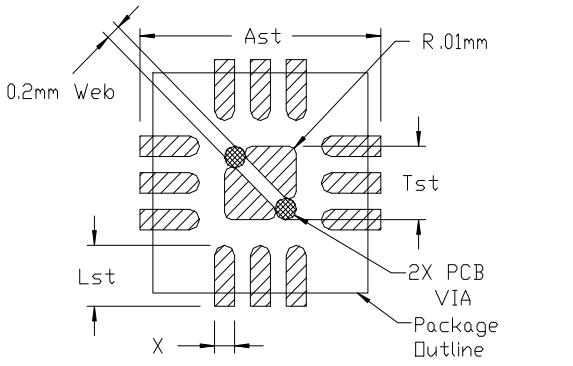
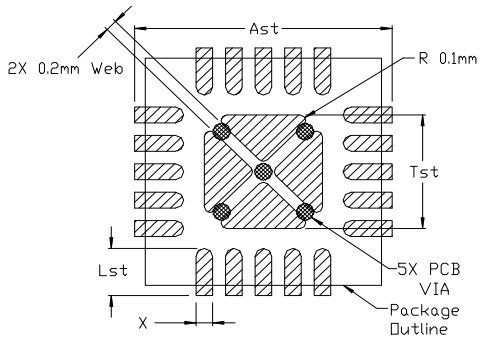
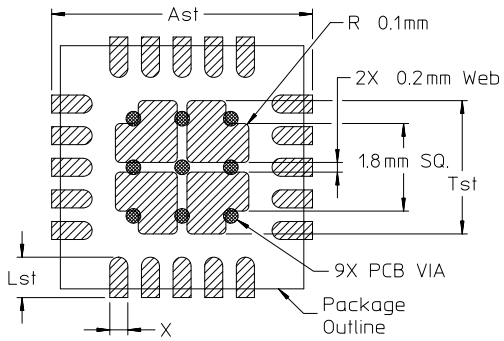
Figure 3-2 Stencil Designs - cont.



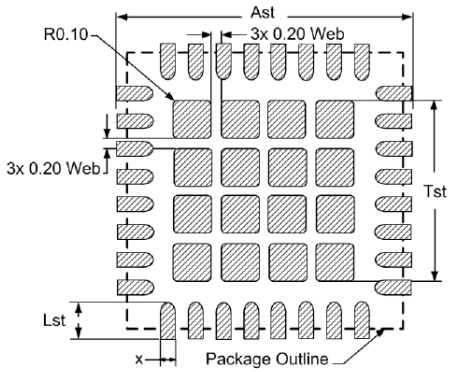
3 mm PQFN



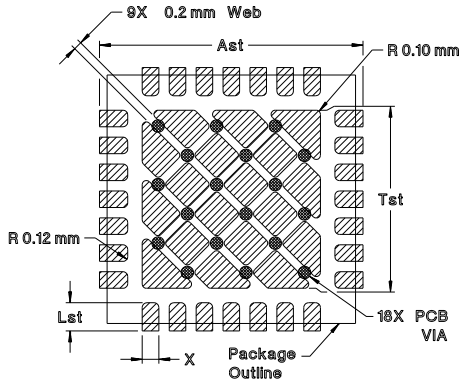
4 mm PQFN



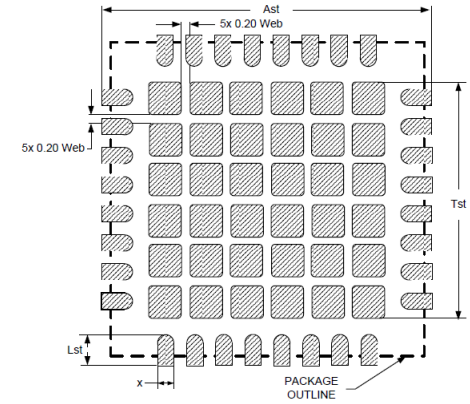
5 mm PQFN



5 mm PQFN 32-LD



6 mm PQFN



7 mm PQFN

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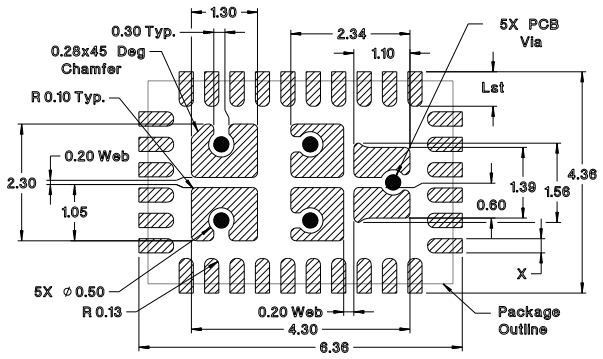
Figure 3-3 Stencil Design



4 x 6 mm PQFN

Table 2. Recommended Solder Mask & Stencil Dimensions

Package			Solder Mask Opening (mm)				Stencil Opening (mm)			
type	mm	leads	Wm	Lm	Tm	Am	X	Lst	Tst	Ast
X1-DFN	1 x 1	6	Fig. 2-2	Fig. 2-2	Fig. 2-2	1.30	0.18	0.35	Fig. 3-1	1.30
TDFN	1.2 x 1.5	6	0.39	0.65	Fig. 2-2	1.56	0.25	0.58	Fig. 3-1	1.56
TDFN	1.5 x 1.2	6	Fig. 2-2	0.565	Fig. 2-2	1.86	0.23	0.495	Fig. 3-1	1.86
PDFN	2 x 2	8	0.42	0.65	Fig. 2-3	2.36	0.28	0.58	Fig. 3-1	2.36
STQFN	2 x 2	12	Fig. 2-3	0.59	0.72	2.36	0.23	0.52	0.62	2.36
STQFN	2 x 2.5	14	Fig. 2-3	0.59	Fig. 2-3	Fig. 2-3	0.23	0.52	Fig. 3-1	Fig. 3-1
LGA	2.25 x 2.25	12	0.34	0.525	0.7 x 0.6	2.61	0.20	0.275	0.6 x 0.5	2.61
LGA	3 x 3	22	0.34	0.500	0.6	3.36	0.20	0.25	0.5	3.36
PQFN	3 x 3	12	0.42	0.90	1.1	3.36	0.28	0.83	1.0	3.36
PQFN	3 x 3 (1.45 mm Exp. Pad)	16	0.42	0.75	1.4	3.36	0.28	0.68	1.3	3.36
PQFN	3 x 3 (1.7 mm Exp. Pad)	16	0.42	0.70	1.5	3.36	0.28	0.63	1.4	3.36
PQFN	4 x 4	16	0.51	0.90	2.1	4.36	0.37	0.83	2.0	4.36
PQFN	4 x 4	20	0.42	0.90	2.1	4.36	0.28	0.83	2.0	4.36
PQFN	4 x 4	24	0.42	0.75	2.45	4.36	0.28	0.68	2.3	4.36
PQFN	4 x 6 (V1)	32	0.42	0.75	Fig. 3-3	Fig. 3-3	0.28	0.68	Fig. 3-3	Fig. 3-3
PQFN	5 x 5 (std)	20	0.51	0.90	3.1	5.36	0.37	0.83	3.0	5.36
PQFN	5 x 5 (Power Amp.)	20	0.51	0.90	3.1	5.36	0.37	0.83	3.0	5.36
PQFN	5 x 5	28	0.42	0.90	3.1	5.36	0.28	0.83	3.0	5.36
PQFN	5 x 5	32	0.42	0.75	3.35	5.36	0.28	0.68	3.25	5.36
PQFN	6 x 6	28	0.54	0.75	4.4	6.36	0.40	0.68	4.3	6.36
PQFN	7 x 7	32	0.51	0.75	5.35	7.36	0.37	0.68	5.25	7.36

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LGA Packages

For large Land Grid Array(LGA) style packages, in order to minimize solder voids on the large ground pad during the SMT attachment process it is recommended that a solder mask be placed on top of the ground pad on the mating PWB. This solder mask grid should have openings that are .035" (0.889 mm) x .035"(0.889 mm) with a .005"(0.127 mm) solder mask web width in the ground pad area. Figure 5 shows the recommended land patterns for various LGA devices. The solder mask grid provides channels for the flux to escape during the reflow process thus minimizing voids and providing a more consistent electrical and thermal path across the device.

In order to achieve minimized voiding a solder paste that is recommended by the solder paste supplier that is for parts that require ultra low voiding should be used. A .004""(.100mm) solder stencil thickness is recommended to reduce the amount of paste being applied and the amount of flux that would need to be burnt off during reflow. In general the aperture openings in the ground pad area are reduced by .003"(.075 mm) around all sides and by .002"(.050 mm) around all sides on the I/O pads. This helps the part to seat properly during reflow. Figure 6 shows the recommended solder stencil for the various LGA devices. When setting up the proper reflow profile, please refer to Tables 3—5 and Figure 7, however extending the soak time towards the higher end of the range(ie 85—90 seconds) will help to start to drive off flux and minimizing voiding in the solder joint.

These same practices outlined above can be applied to other LGA style packages.

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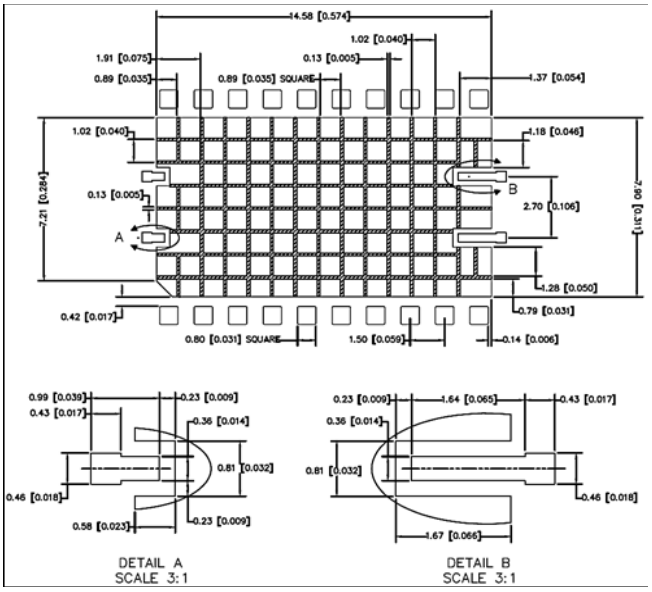
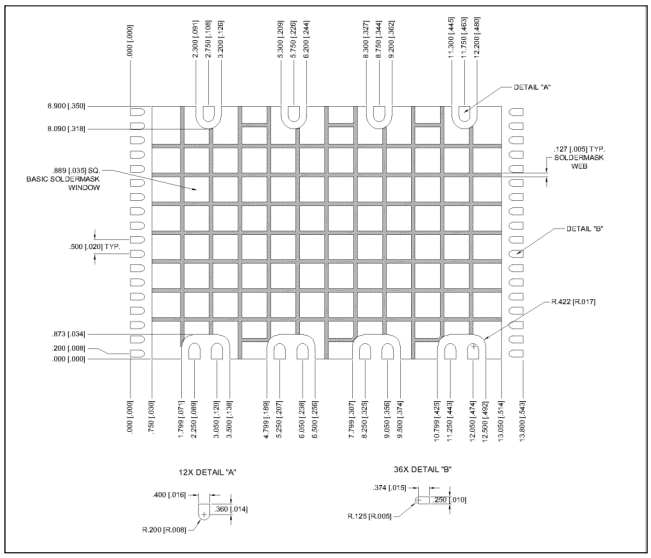
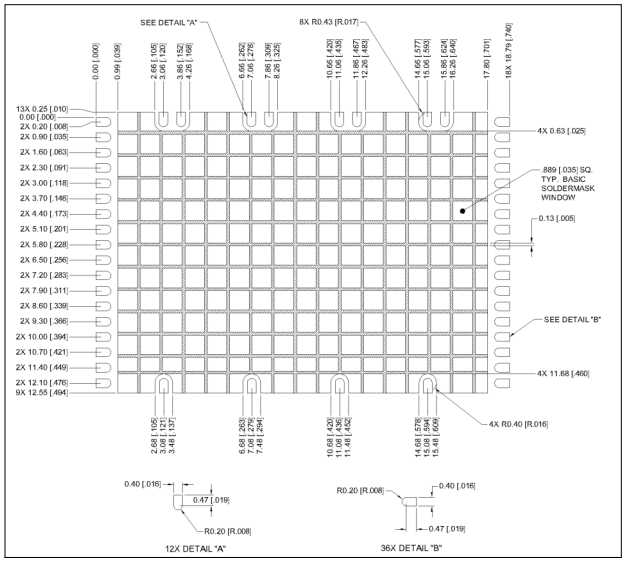
Figure 5: Land and Solder Mask Layouts



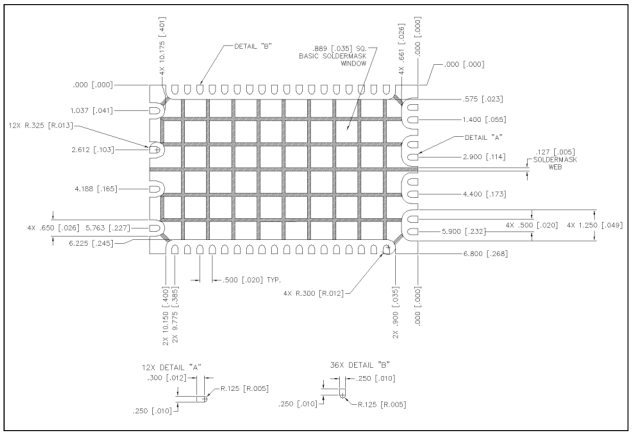
16.1 x 10.6 mm



14.0 x 9.1 mm



19.0 x 13.0 mm



11.0 x 7.0 mm

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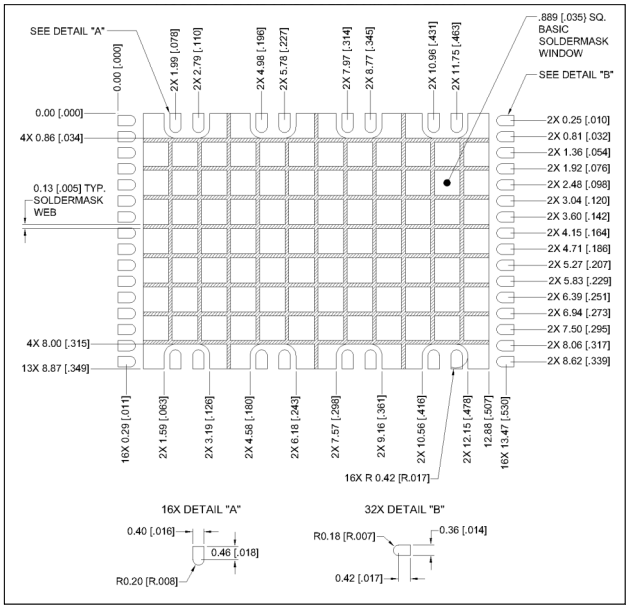
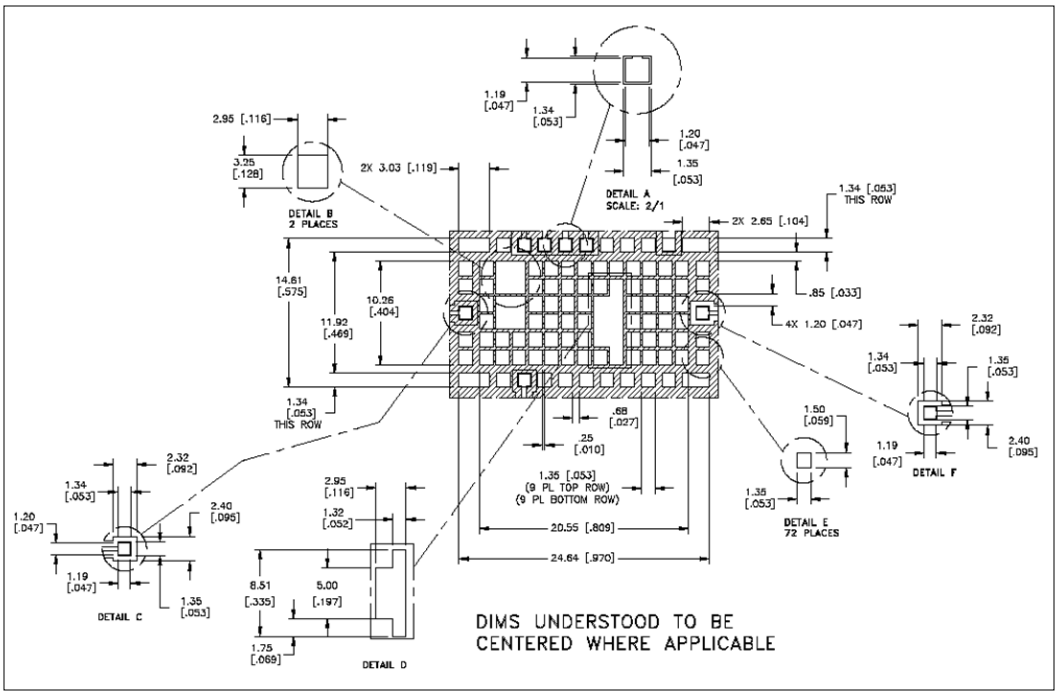
Figure 5: Land and Solder mask Layouts Cont'd



14.0 x 9.1 mm



14.0 x 24.0 mm

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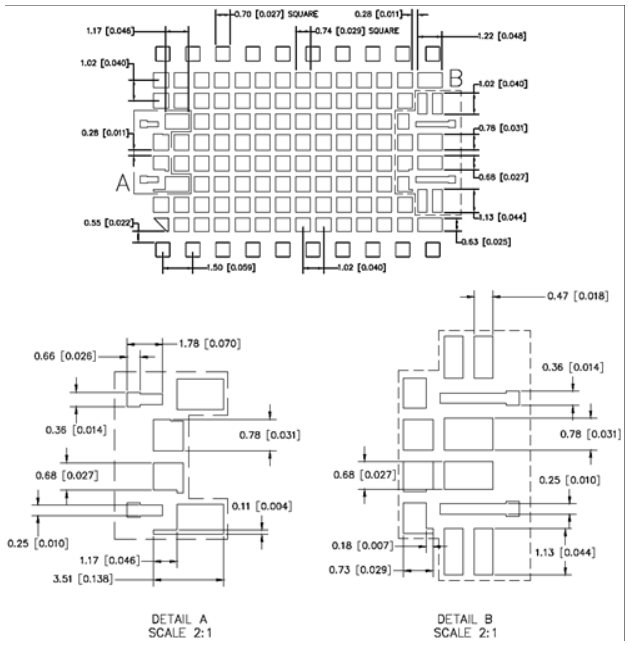
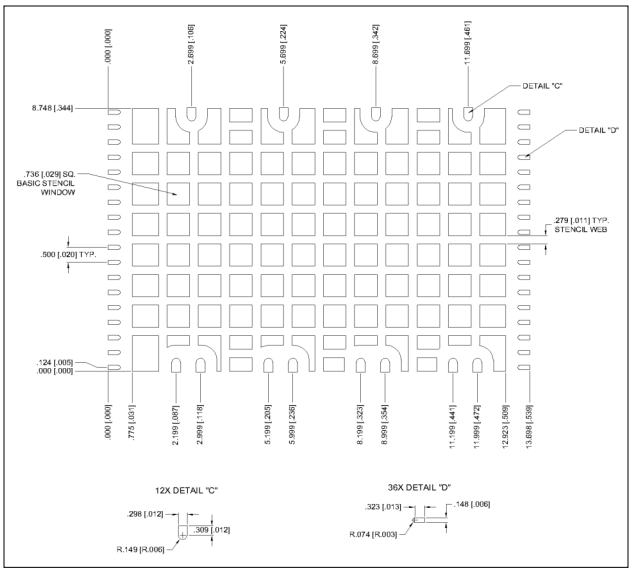
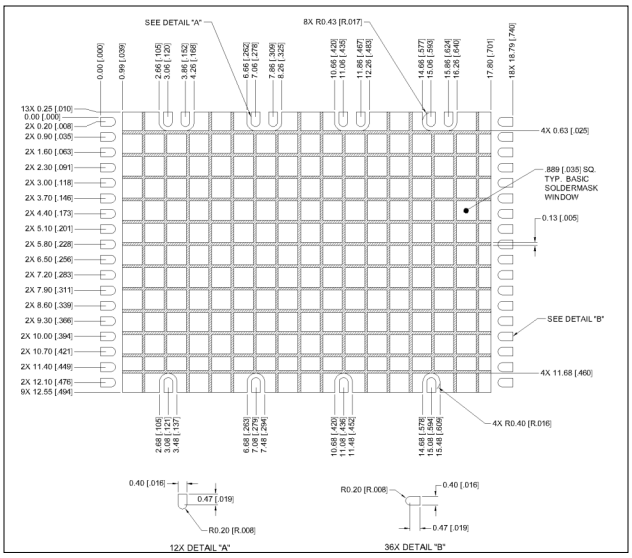
Figure 6: LGA Stencil Designs



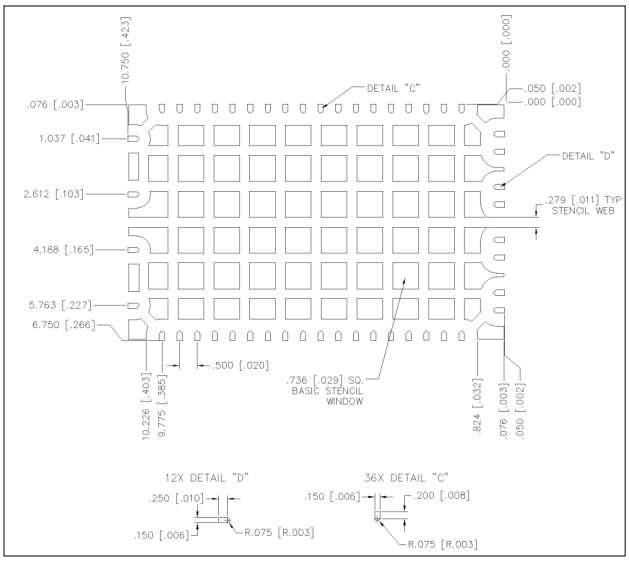
16.1 x 10.6 mm



14.0 x 9.1 mm



19.0 x 13.0 mm



11.0 x 7.0 mm

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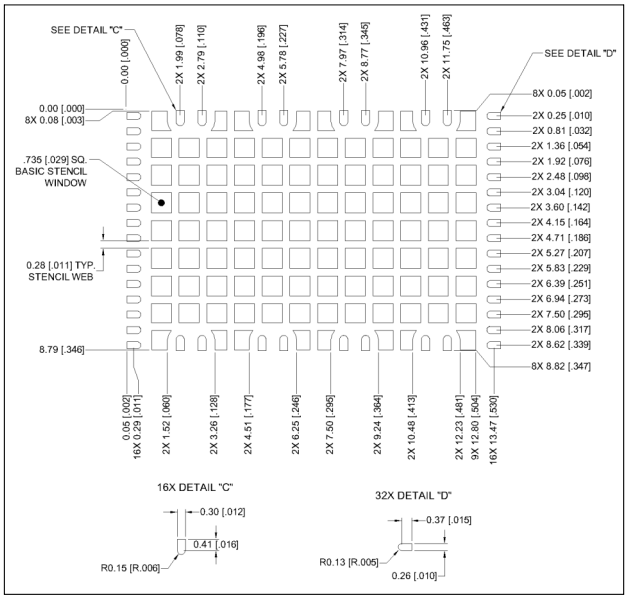
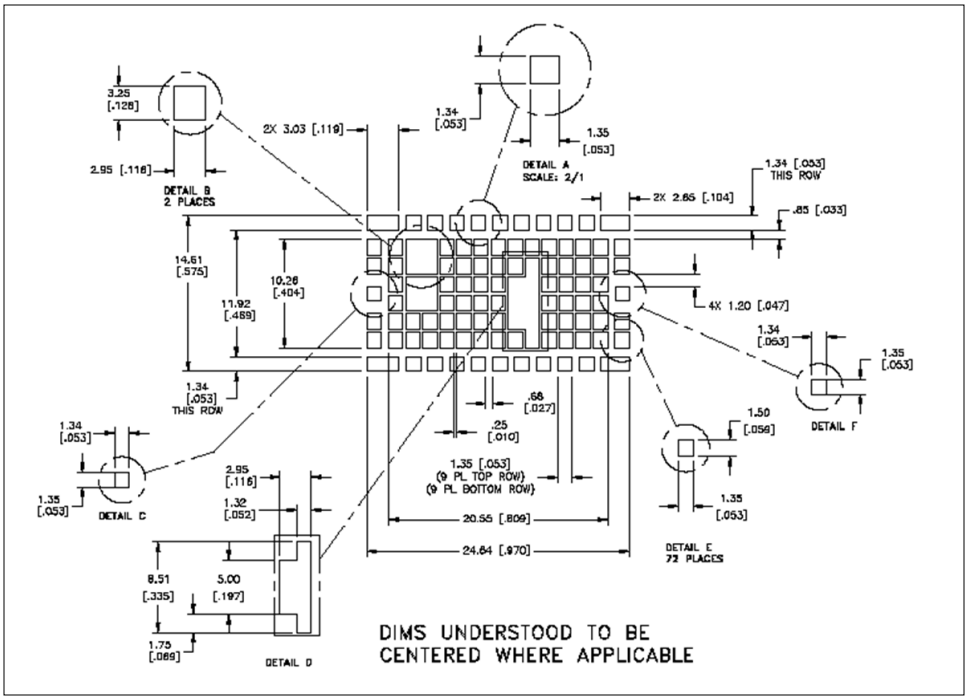
Figure 6: LGA Stencil Designs Cont'd



14.0 x 9.1 mm



14.0 x 24.0 mm

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Surface Mount Instructions for QFN / DFN and LGA Laminate Packages

Reflow Profile

The most common solder reflow method is accomplished in a belt furnace using convection heat transfer. Tables 3 thru 5 along with Figure 4 show a typical convection reflow profile of temperature versus time. The profile reflects the three distinct heating stages, or zones (preheat, reflow, and cooling) recommended in automated reflow processes to ensure reliable, finished solder joints. The profile will vary among soldering systems and is intended as an example to use as a starting point. Other factors that can affect the profile include the density and types of components on the board, type of solder used and type of board or substrate material being used.

Thermocouples should be securely attached to the top surface of a representative component to insure the temperature exposure is met. Profile should be recorded by data acquisition for future reference.

General Soldering Precautions

The melting temperature of solder generally exceeds the recommended maximum operating temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, always observe the following instructions to minimize the thermal stress to the devices.

- Always preheat the device (failure to do so can cause excessive thermal shock and stress that can result in damage to the device).
- Limit the temperature in the reflow stage to peak temperature indicated in Tables 3 thru 5.
- After completing the soldering process, allow the devices to cool naturally for at least 3 minutes. Gradual cooling should be used, as the use of forced cooling will increase the temperature gradient and may result in latent failure due to mechanical stress.
- Avoid any mechanical stress or shock to the solder joints and devices during cooling.

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Table 3. Reflow Conditions

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (Ts_{min}) Temperature Max (Ts_{max}) Time (t_s) from (Ts_{min} to Ts_{max})	 100°C 150°C 60 - 120 seconds	 150°C 200°C 60 - 120 seconds
Ramp-Up Rate (T_L to Tp)	3°C/second max.	3°C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183°C 60 - 150 seconds	217°C 60 - 150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the Classification temperature in Table 4 For suppliers Tp must not exceed the Classification temperature in Table 4	For users Tp must not exceed the Classification temperature in Table 5 For suppliers Tp must not exceed the Classification temperature in Table 5
Time (tp)* within 5 °C of the specified Classification temperature (T_C), see re-flow profile	20* seconds	30* seconds
Ramp-Down Rate (Tp to T_L)	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum		

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), T_p **shall** be within ± 2°C of the live-bug T_p and still meet the T_c requirements, otherwise, the profile **shall** be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.
Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table 3
For example, if T_c is 260°C and time t_p is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.
Note 3: All components in the test load **shall** meet the classification profile requirements.
Note 4: SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.

Table 4. SnPb Eutectic Process - Classification Temperature (T_C)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235°C	220°C
≥2.5 mm	220°C	220°C

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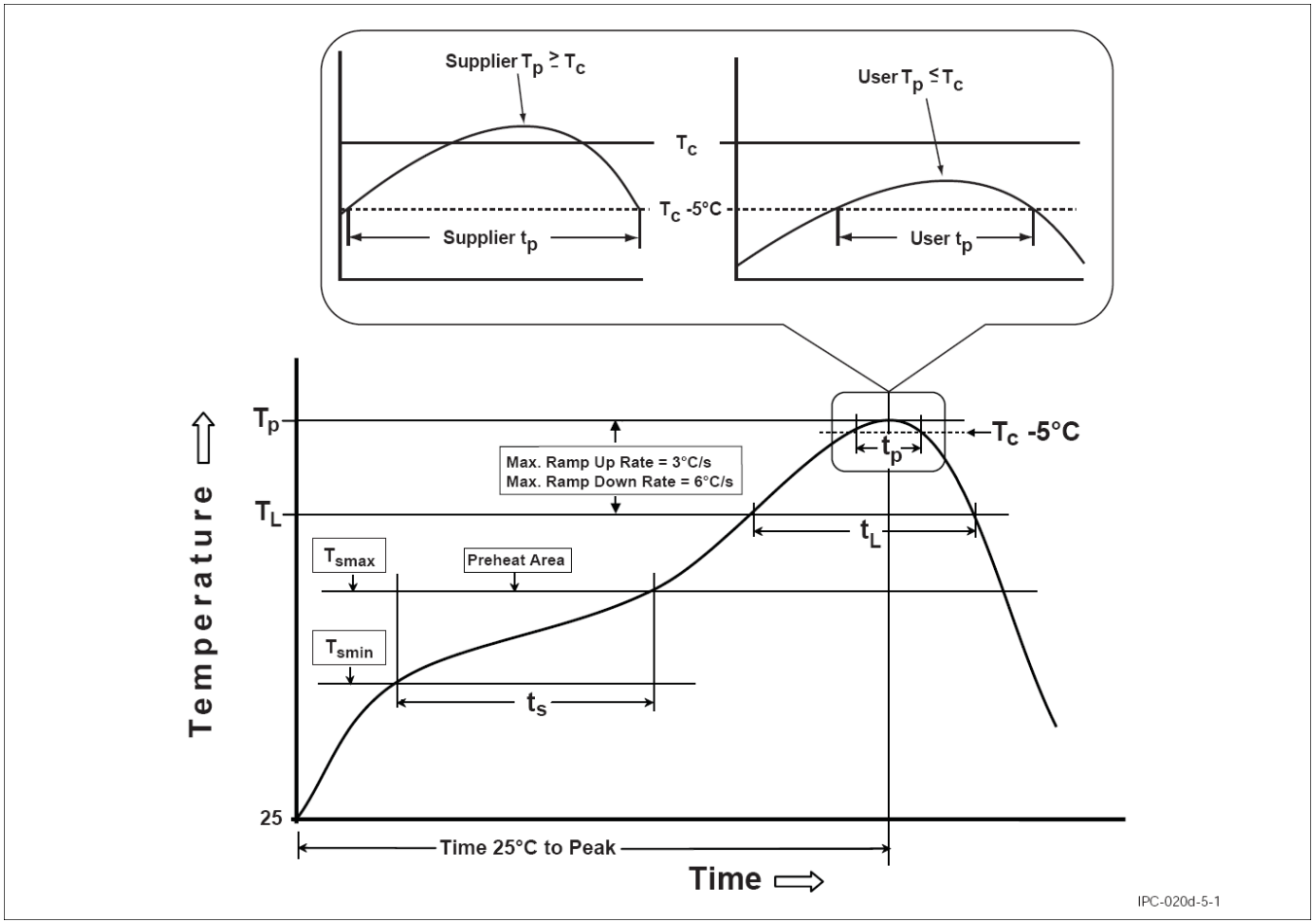
Table 5. Pb-Free Process - Classification Temperature (T_C)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm - 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Note 1: At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (T_p) can exceed the values specified in Tables 4 or 5. The use of a higher T_p does not change the classification temperature (T_c).
Note 2: Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.
Note 3: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.
Note 4: Moisture sensitivity levels of components intended for use in a Pb-free assembly process **shall** be evaluated using the Pb-free classification temperatures and profiles defined in Tables 3 and 5, whether or not Pb-free.
Note 5: SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired

Figure 7. Reflow Profile



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